METHOD OF FABRICATING W/TiN GATE FOR MOSFETS

Field of Invention

The present invention relates to a semiconductor device, and more specifically, to a method of fabricating a metal oxide semiconductor field effect transistor (MOSFET) for used in deep sub-micron meter range.

Background of the Invention

The semiconductor industry has been advanced in an ever brisk pace, recently. In order to achieve high performance integrated circuits or high package density of a wafer, the sizes of semiconductor devices have become smaller and smaller than before in the field of Ultra Large Scale Integrated (ULSI) technologies. The semiconductor industry has been advanced to the field of Ultra Large Scale Integrated (ULSI) technologies. The fabrication of the metal-oxide-semiconductor transistor also follows the trend. As the size of the devices is scaled down, silicon based nano-scale electronics have been attention for these years. For example, single-electron-tunneling devices are developed in recent years.

Integrated circuits includes more than millions devices in a specific area of a wafer and electrically connecting structure for connecting these devices to perform desired function. One of the typical devices is metal oxide semiconductor field effect transistor (MOSFET). The MOSFET has been widely, traditionally applied in the semiconductor technologies. As the trend of the integrated circuits, the fabrication of the MOSFET also meets various issues to

fabricate them. The typically issue that relates to hot carriers injection is overcame by the development of lightly doped drain (LDD) structure.

Further, the requirement of the devices towards high operation speed and low operation power. For deep sub-micron meter MOS devices, the self-aligned silicide (SALICIDE) contact, ultra-shallow source and drain junction are used for improving the operation speed and short channel effect. In another research by T. Yoshitomi, he develops a high performance CMOS with good control of short channel effect and silicide resistance. Please see "High Performance 0.15 μm Single Gate Co Salicide CMOS, T. Yoshitomi et al., 1996, Symposium on VLSI Technology Digest of Technical papers". The $CoSi_2$, NiSi have been used for deep sub-micron high speed CMOS due to the low sheet resistance of fine silicide line. However, it is difficult to make ultra-shallow junction and form SALICIDE contact without degrading the device performance.

The requirement of the ULSI CMOS technology is the need of devices operated at low supply voltage and they have high speed. When the supply-voltage is reduced, the threshold voltage needs to be scaled down to achieve the desired circuit switching speed. IBM has proposed that CMOS employs non-uniform channel doping profiles and ultra-shallow source and drain extensions and halos, which can be referenced in "CMOS technology scaling 0.1 μm and beyond, IBM semiconductor research and development center, Bijan Davari, 1996, IEDM, 96-555". For the high performance case, the threshold voltage is scaled down less than the supply voltage in order to maintain a reasonable standby current.

US Patent No. 6,261,934 which assigned to Texas Instruments Incorporated (Dallas, TX), entitled "Dry etch process for small-geometry metal gates over thin gate dielectric" discloses a structure for semiconductor device. As geometries shrink into the deep submicron regime (below 0.5 or 0.35 micron), such buried channels become very undesirable. Thus one of the constraints on new gate materials is a good work-function match to the semiconductor used. Titanium nitride is a very promising candidate for gate electrode material. It has a work function near the mid-gap point of silicon (4.65 eV) and eliminates gate depletion effects. However, titanium nitride has a quite high resistivity (120 m.OMEGA.-cm), and therefore needs to be used in conjunction with a material with higher conductivity for low interconnect delays to be achieved. For that purpose, tungsten (resistivity of 8 m.OMEGA.-cm) has been used.

Summary of the Invention

The method of the present invention includes forming a dielectric layer on said semiconductor substrate. A dielectric layer is etched to form an opening in dielectric layer. A gate oxide layer is formed on semiconductor substrate in said opening. A barrier conductor is formed along the surface of the opening. A metal layer is formed on the barrier conductor and refilled into the opening. A portion of the metal layer and the barrier conductor is removed to form a gate for said transistor. The dielectric layer is removed. The barrier conductor is removed on sidewall of the gate. Lightly doped drain region is formed in the semiconductor substrate. Next, Sidewall spacer is formed on sidewall of the gate. Then, source

and drain is formed in the semiconductor substrate by ion implantation using the gate and spacer as masking.

Brief Description of the Drawings

The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIGURE 1 is a cross section view of a semiconductor wafer illustrating the steps of forming a dielectric layer, a barrier conductor and metal layer on a semiconductor substrate according to the present invention.

FIGURE 2 is a cross section view of a semiconductor wafer illustrating the step of forming a gate structure according to the present invention.

FIGURE 3 is a cross section view of a semiconductor wafer illustrating the step of removing the dielectric layer according to the present invention.

FIGURE 4 is a cross section view of a semiconductor wafer illustrating the step of removing the TiN according to the present invention.

FIGURE 5 is a cross section view of a semiconductor wafer illustrating the step of forming LDD and source and drain according to the present invention.

FIGURE 6 is a cross section view of a semiconductor wafer illustrating another structure according to the present invention.

Detailed Description of the Preferred Embodiment

The present invention proposes a novel method to fabricate a W/Si gate for MOSFETS. In the present invention, the technology can increase the device performance.

In a preferred embodiment, a single crystal silicon substrate 2 with a <100> crystallographic orientation is provided. Thick field oxide (FOX) regions or shallow trench isolation are formed to provide isolation between devices on the substrate. In a case, the FOX regions can be formed via lithography and etching steps to etch a silicon nitride-silicon dioxide composition layer. After the photoresist is removed and wet cleaned, thermal oxidation in steam environment is used to grow the FOX regions 4 to a thickness of about 3000-8000 angstroms. The FOX regions 4 can be replaced by a plurality of shallow trench isolations, as well known in the art.

A first dielectric layer 4 is then formed over the substrate 2 using a low-pressure chemical vapor deposition process. In preferred embodiment, the first dielectric layer 4 is formed of oxide, nitride, oxynitride or the combination thereof. Turning to FIGURE 1, next, standard lithography and etching steps are used to etch the first dielectric layer 4 to form an opening 5 for exposing the substrate 2. The gate oxide layer 6 is formed after the step by thermal oxidation. A silicon dioxide layer 6 is formed on the top surface of the substrate 2 to serve as a gate oxide of a subsequently formed MOSFET. Typically, the silicon dioxide layer 6 is formed in an oxygen ambient at a temperature of about 800 to 1100 centigrade degrees. In the embodiment, the thickness of the

silicon dioxide layer 6 is approximately 15-250 angstroms. Alternatively, the oxide layer 6 may be formed using any suitable oxide chemical compositions and procedures, such as chemical vapor deposition.

Subsequently, a barrier conductor (Titanium nitride) 8 is formed on the first dielectric layer 4 and along the surface of the opening 5, preferably, the barrier conductor 8 is formed of TiN. Then, a metal layer 10 is formed on the barrier conductor 8 and refilled into the opening 5. In a preferred embodiment, the metal layer 10 is formed of titanium, tungsten, aluminum, or copper.

Next, a chemical mechanical polishing is used to remove the barrier conductor 8 and metal layer 10 to the surface of the first dielectric layer 4 for forming the gate, as shown in FIGURE 2.

Turning to FIGURE 3, the first dielectric layer 4 is removed by hot phosphorus, BOE or HF solution depending on the material for forming the first dielectric layer 4. An isotropical etching is used to remove the Titanium nitride 8 attached on the tungsten gate 10 as shown in FIGURE 4. The plasma-etching recipe may include O_2+C_2F_6. US Patent No. 6,261,934 disclosed the method to etch the Titanium nitride 8. The step may be omitted. If the TiN does not be removed, oblique (titled) angle ion implantation such as LATIPS (large tilt-angle implanted punch-through stopper) may be used for forming the LDD.

Please turn to FIGURE 5, lightly doped drain regions 12 are formed by using ion implantation. Next, spacer 14 is formed on the sidewall of the gate 10. The step can be achieved by forming a dielectric layer then etching the layer. Finally, source and drain 16 are created by ion implantation using the gate 10 and space 14 as the masking.

Another structure after the sidewall TiN is striped is shown in FIGURE 6. It has to be noted that the structure include under cut portion 11 under the gate 10. After the spacer is formed, the LDD structure may be formed by using oblique rotation ion implantation such as LATIPS (large tilt-angle implanted punch-through stopper) technique. The LATIPS transistor employs a large tilt-angle implanted punch-through stopper (LATIPS). This implant forms higher concentration doped regions under the gate to prevent bulk punch-through.

As will be understood by persons skilled in the art, the foregoing preferred embodiment of the present invention is illustrative of the present invention rather than limiting the present invention. Having described the invention in connection with a preferred embodiment, modification will now suggest itself to those skilled in the art. Thus, the invention is not to be limited to this embodiment, but rather the invention is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar structures. While the preferred embodiment of the invention has been illustrated and described, it will be appreciated that various changes can be

made therein without departing from the spirit and scope of the invention.